REMARKS

The present Amendment is in response to the Examiner's Office Action mailed April 27, 2005. Claims 26, 34, 37, 42, 43, and 55 are amended. Claims 26-60 are now pending in view of the above amendments.

Reconsideration of the application is respectfully requested in view of the above amendments to the claims and the following remarks. For the Examiner's convenience and reference, Applicants' remarks are presented in the order in which the corresponding issues were raised in the Office Action.

Please note that the following remarks are not intended to be an exhaustive enumeration of the distinctions between any cited references and the claimed invention. Rather, the distinctions identified and discussed below are presented solely by way of example to illustrate some of the differences between the claimed invention and the cited references. [1] In addition, Applicants request that the Examiner carefully review any references discussed below to ensure that Applicants' understanding and discussion of the references, if any, is consistent with the Examiner's understanding. Also, Applicants' arguments related to each cited reference are not an admission that the cited references are, in fact, prior art.

I. Objections to the Claims

The Examiner objects to claims 34, 37, 43, and 55 for various typographical errors. In response, claims 34, 37, 43, and 55 are amended as suggested by the Examiner and the removal of this rejection is respectfully requested.

II. Rejection Under 35 U.S.C. §102(e)

The Examiner rejects claims 26-28, 33, and 40 under 35 U.S.C. § 102(e)[2] as being anticipated by *Takushima* (United States Patent No. 6,454,159). Applicants respectfully traverse this rejection on the grounds that *Takushima* does not disclose each feature of the presently recited claims.

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[1] In addition to the following remarks, Applicants incorporate by reference its previous arguments made as to the patentability of these and all other pending claims.

[2] Because *Takushima* is only citable under 35 U.S.C. § 102(e) Applicants do not admit that *Takushima* is in fact prior art to the claimed invention but reserve the right to swear behind *Takushima* if necessary to remove it as a reference.

Takushima teaches a method for forming a solder bump. The method includes, among other things: (1) forming a plurality of distinct recesses in a solder plate; (2) filling the distinct recesses with solder; (3) carefully aligning a plurality of core bumps of an electronic component with respective recesses in the solder plate; and (4) then dipping the plurality of core bumps into the respective properly aligned distinct recesses. *See e.g.* Abstract; col. 2, lines 58-63; col. 3, lines 57-60; col. 4 lines 37-40 and 63-67; Figs. 1(a)-1(c). This is a relatively intensive effort, analogous to applying the solder with the help of a mask because the recesses must be carefully formed, preferably by photolithography, and the solder must be carefully inserted into each recess. Col. 3, lines 60-62. Because of these distinct recesses, careful alignment between the core bumps and the recesses must be made. *See* column 4, lines 35-38 ("[R]espective core bumps 14 on chip 10 are brought into contact with respective quantities of solder in recesses 18 in plate 16. In this case, a highly precise mounting machine is preferably used.")

In direct contrast, present independent claim 26 specifically recites, *inter alia*: "bringing the entire interconnection surface in contact with molten solder, wherein the solder selectively wets and adheres to the cores but not to the non-wetting surface, thereby depositing solder on all of the cores to form solder bumps thereon and leaving a substantial absence of solder between cores." As noted in the application as filed in paragraph 24: "The projecting...studs thus formed on the contact pads 2 are then brought into contact with molten solder, for example by dipping in a solder bath, whereupon it is found that the solder selectively wets and adheres only to the studs and not to the other areas of the semiconductor chip." In some embodiments of the invention a wave solder process can also be used. Regardless, a mask is not needed because solder is applied to the entire interconnection surface, including the cores and other areas of the semiconductor chip, but only adheres to the cores. Precise alignment is also not needed because the inventive methods are self aligning. *See* paragraph [0024] ("This selective wetting of the metal studs by the solder effectively self aligns the solder without the need for any additional alignment steps.")

This is directly contrary to *Takushima's* use of recesses for holding solder wherein the cores must be carefully aligned and precisely dipped in the recesses such that solder does not contact the rest of the chip.

Accordingly, Applicants respectfully submit that *Takushima* does not teach or suggest the limitations of present claim 26. Claims 27, 28, 33, and 40 depend from claim 26 and therefore

contain the limitations therein. Claims 27, 28, 33, and 40 are therefore not anticipated by *Takushima* for at least the same reasons as claim 26. Since *Takushima* does not teach the method of claims 26-28, 33, and 40, Applicants respectfully request that the rejection of these claims under 35 U.S.C. § 102(e) be withdrawn.

III. Rejection Under 35 U.S.C. § 103

The Examiner variously rejects claims 29-32, 34-39, and 41-60 under 35 U.S.C. § 103 as being unpatentable over *Takushima* and in view of one or more of *Lin* (United States Patent No. 6,440,835), *Azdasht et al.* (United States Patent No. 6,043,985), *Gutierrez* (United States Patent No. 6,395,983), *Cotte et al.* (United States Patent No. 6,281,105), and *Abbott et al.* (United States Patent No. 6,337,445).

Applicants traverse the Examiner's rejections for obviousness on the grounds that the references – either individually or in combination – fail to teach or suggest each and every element of the rejected claims. By contrast to the presently claimed invention, *Takushima* does not teach or suggest "bringing the entire interconnection surface in contact with molten solder, wherein the solder selectively wets and adheres to the cores but not to the non-wetting surface, thereby depositing solder on all of the cores to form solder bumps thereon and leaving a substantial absence of solder between cores," as is presently claimed in the independent claim 26. Claims 42 and 55 recited similar features of the invention. None of *Lin*, *Azdasht*, *Gutierrez*, *Cotte*, and *Abbott* can overcome the foregoing deficiencies of *Takushima* because they fail to teach of suggest the above feature of the invention.

Accordingly, in view of the failure of the references to teach a method for contacting cores to molten solder as presently claimed, Applicants submit that the Examiner has failed to set forth a *prima facie* case for obviousness for the independent claims 26, 42, and 55. Claims 29-32, 34-39, 41, 43-54, and 56-60 depend from claim 26, 42, or 55 and therefore contain the limitations therein. Claims 29-32, 34-39, 41, 43-54, and 56-60 are therefore not obviated by the cited references for at least the same reasons as the parent independent claims. The Applicants therefore respectfully request that the foregoing rejections under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

In view of the foregoing, Applicants believe the claims as amended are in allowable form. In the event that the Examiner finds remaining impediment to a prompt allowance of this application that may be clarified through a telephone interview, or which may be overcome by an Examiner's Amendment, the Examiner is requested to contact the undersigned attorney.

Dated this 24th day of June, 2005.

Respectfully submitted,

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